CLAIMS

What is claimed is:

1. A method for controlling a bandwidth of an analog filter circuit comprising:

performing a DC offset correction operation in the analog filter circuit to generate a DC offset correction signal;

holding the DC offset correction signal in the analog filter circuit;

adding a training signal to the DC offset correction signal;

determining a magnitude of a filtered input signal using the training signal and the DC offset correction signal;

determining a magnitude of the filtered input signal at a predetermined frequency using the training signal and the DC offset correction signal;

determining a difference between the magnitudes of the filtered input signal and the filtered input signal at the predetermined frequency;

comparing the difference to a predetermined threshold value to generate an error metric; and

using the error metric to adjust the bandwidth frequency of the analog filter circuit.

2. The method of claim 1, wherein determining a magnitude of a filtered input signal further comprises:

low pass filtering the filtered input signal to generate a low pass filtered signal; and

determining a magnitude of the low pass filtered signal.

3. The method of claim 1, wherein determining a magnitude of a filtered input signal at the predetermined frequency further comprises:

mixing the filtered input signal with a sinusoidal signal at the predetermined frequency to produce a baseband signal;

low pass filtering the baseband signal around the predetermined frequency to produce a low pass filtered input signal located at the predetermined frequency; and

determining a magnitude of the low pass filtered input signal at the predetermined frequency.

4. The method of claim 1, wherein the predetermined frequency is a bandwidth frequency equal to about the -3 dB (decibel) corner of the analog filter.

5. The method of claim 1, further comprising filtering the error signal using a loop filter having a predetermined bandwidth.

6. The method of claim 1, wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being used to adjust the bandwidth of the analog filter circuit.

7. The method of claim 1, wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being used to adjust pole and zero locations of the analog filter circuit.

8. The method of claim 1, wherein the error metric is used to select filter coefficients from a look-up table, the filter coefficients being provided to the analog filter circuit on a multi-bit bus.

9. The method of claim 1, wherein the training value is generated using a pseudo-random sequence generator.

10. The method of claim 1, wherein the analog filter circuit is an active resistor-capacitor (RC) filter.

11. The method of claim 1, wherein the analog filter circuit is a gm-C type filter.

12. The method of claim 1, wherein the method is performed in a spread spectrum code-division multiple access (CDMA) receiver.

13. The method of claim 1, wherein the method is performed in a spread spectrum code-division multiple access (CDMA) transmitter.

14. A filter circuit comprising:

an analog filter element having an input for receiving an analog input signal, an output for providing a filtered output signal, and a control input for receiving a control signal for adjusting a bandwidth frequency of the analog filter element to a predetermined bandwidth frequency;

an analog-to-digital converter having an input coupled to the output of the analog filter element, and an output;

a digital tracking loop having an input coupled to the output of the analog-to-digital converter, and an output coupled to the control input of the analog filter element, the digital tracking loop for comparing a magnitude difference to a predetermined threshold to generate an error signal, the error signal used to generate the control signal, where the magnitude difference is determined by subtracting a first magnitude of the analog input signal over a predetermined frequency range to a second magnitude of the analog input signal over the predetermined frequency range.

15. The filter circuit of claim 14, wherein the analog filter element is characterized as being an active-RC (resistor-capacitor) filter element.

16. The filter circuit of claim 14, wherein the digital tracking loop further comprises:

a first low pass filter having an input coupled to the output of the analog-to-digital converter, and an output;

a first magnitude determination unit having an input coupled to the output of the low pass filter, and an output for providing the first magnitude of the analog input signal;

a mixer circuit having an input coupled to the output of the analog-to-digital converter, and an output;

a second low pass filter having an input coupled to the output of the mixer circuit, and an output;

a second magnitude determination unit having an input coupled to the output of the second low pass filter, and an output for providing the second magnitude of the analog input signal over the predetermined frequency range located approximately at the predetermined bandwidth frequency;

a summation element having an input for receiving the first and second magnitudes, and an output for providing the magnitude difference; and

a comparator having a first input for receiving the magnitude difference, a second input for receiving the predetermined threshold, and an output for providing the error signal.

17. The filter circuit of claim 16, further comprising:

a loop filter with programmable loop bandwidth having an input coupled to the output of the comparator, and an output; and

a look-up table having an input coupled to the loop filter, and an output for providing the control signal to the control input of the analog filter element.

18. The filter circuit of claim 16, further comprising a numerically controlled oscillator for providing a sinusoidal signal located approximately at the bandwidth frequency of the analog filter to the mixer circuit.

19. The filter circuit of claim 16, wherein the look-up table includes values for controlling pole and zero locations of the analog filter element.

20. The filter circuit of claim 14, further comprising:

a DC offset correction circuit having an input coupled to the output of the analog-to-digital converter, and an output;

a first summation circuit having a first input coupled to the output of the DC offset correction circuit, a second input, and an output;

a digital-to-analog converter having an input coupled to the output of the summation circuit, and an output; and

a second summation circuit having a first input coupled to the output of the digital-to-analog converter, a second input for receiving an analog signal, and an output coupled to the input of the analog filter element.

21. The filter circuit of claim 20, further comprising:

a random number sequence generator having an input coupled to the second input of the first summation circuit.

22. The filter circuit of claim 21, wherein the random number sequence generator is for generating a pseudo-random number sequence.

23. The filter circuit of claim 20, further comprising single or multiple sinusoidal tones generator having an input coupled to the second input of the first summation circuit.

24. The filter circuit of claim 14, wherein the filter circuit is used in a spread spectrum code-division multiple access (CDMA) receiver.

25. The filter circuit of claim 14, wherein the filter circuit is used in a spread spectrum code-division multiple access (CDMA) transmitter.

26. A filter circuit comprising:

an analog filter element having an input for receiving an analog input signal, an output for providing a filtered output signal, and a control input for receiving a control signal for adjusting a bandwidth frequency of the analog filter element to a predetermined bandwidth frequency;

an analog-to-digital converter having an input coupled to the output of the analog filter element, and an output;

a digital tracking loop having an input coupled to the output of the analog-to-digital converter, and an output coupled to the control input of the analog filter element, the digital tracking loop for comparing a magnitude difference to a predetermined threshold to generate an error signal, the error signal used to generate the control signal, where the magnitude difference is computed by subtracting a magnitude of an analog input signal over a predetermined frequency range approximately at the analog filter's center frequency to a magnitude of the analog input signal over a predetermined frequency range approximately at the bandwidth frequency of the analog filter.